Code No: R22023 **R10** SET - 1

II B.Tech II Semester, Regular Examinations, April – 2012
SWITCHING THEORY AND LOGIC DESIGN
(Com. to EEE, ECE, BME, EIE, ECC)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Assume an arbitrary number system having a radix of 5 and 0, 1, 2, L and M as its independent digits. Determine:
   i) The decimal equivalent of (2LM.L1)
   ii) The octal equivalent of (21L.M2)
   iii) The hexagonal equivalent of (LM1.L2)
   iv) The total number of possible four-digit combinations in this arbitrary number system.
   b) What is an excess-3 BCD code? Which short coming of the 8421 BCD code is overcome in the excess-3 BCD code? Illustrate with the help of an example. (8M+7M)

2. a) i) Simplify $F(A,B,C,D,E) = AB\overline{C}\,\overline{D} + AB\overline{C}D + A\overline{B}CD + ABCDE + AB\overline{C}\,\overline{D}\,\overline{E} + AB\overline{C}DE$
   ii) Prove that $[A\overline{B} + \overline{C} + \overline{D}][D + (E + \overline{F})G] = D(A\overline{B} + \overline{C}) + \overline{D}G(E + \overline{F})$
   b) With the help of the generalized form of the Hamming code, explain how the number of parity bits required to transmit a given number of data bits (8M+7M)

3. a) Write a simplified max-term Boolean expression for Π 0, 4, 5, 6, 7, 10, 14 using the Karnaugh mapping method.
   b) Minimize the following function using the Quine-McCluskey method.
   Y = ∑(1, 2, 5, 8, 9, 10, 12, 13, 16, 18, 24, 25, 26, 28, 29, 31) (6M+9M)

4. a) Discuss the functional principle of 4-bit ripple carry adder what is its major disadvantage?
   b) Draw the logic diagram of a three-digit Excess-3 adder and briefly describe its functional principle? (8M+7M)

5. a) Design a two-level positive logic decimal-to-BCD priority encoder for decimal inputs from 0 to 4.
   b) Implement the following logic function using MUX with three select inputs? (8M+7M)
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6. a) Obtain the programming table for three-digit binary to gray code conversion using PLA
   b) How does a programmable logic device differ from a fixed logic device? What are the primary advantages of using programmable logic devices? (8M+7M)

7. a) Design a synchronous counter that counts as 000, 010, 101, 110, 000, 010 … Ensure that the un used states of 001, 011, 100 and 111 go to 000 on the next clock pulse. Use J-K flip-flops.
   b) Obtain conversion from D flip-flop to J-K flip-flop (9M+6M)

8. Derive a circuit that realizes the FSM defined by the state assigned table below using JK flip-flops (15M)

PS	NS, Z	
	X=0	X=1
A	B,0	E,0
B	E,0	D,0
C	D,1	A,0
D	C,1	E,0
E	B,0	D,0

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1. a) Perform the following operations using r-1's complement arithmetic:
   i) $(+43)_{10} - (-53)_{10}$.
   ii) $(3F85)_{16} - (1E73)_{16}$
   b) Prove that16-bit 2's complement arithmetic cannot be used to add +18150 and +14618, while it can be used to add −18150 and −14618. (8M+7M)

2. a) What do you understand by canonical and expanded forms of Boolean expressions? Illustrate with examples.
   b) What is the Hamming distance? Discuss with the help of examples, what is the role of the Hamming distance in deciding the error detection and correction capability of a code meant for the purpose? (8M+7M)

3. a) i) Simplify the Boolean function given by
   $f(X,Y,Z) = X.Z + \overline{X}.\overline{Z}$ for the don't care condition expressed $X.\overline{Y} + X.Y.\overline{Z} + \overline{X}.\overline{Y}.Z$ as
   ii) Simplify the Boolean function given by
   $f(A,B,C) = (A+B+C)(\overline{A}+B+C)(A+\overline{B}+C)$for the don't care condition expressed as $(\overline{A}+\overline{B})(\overline{A}+B+C)$
   b) Minimizing a given Boolean expression using the Quine–McCluskey tabular method yields the following prime implicants: −0−0, −1−1, 1−10 and 0−00. Draw the corresponding Karnaugh map. (9M+6M)

4. a) How can a 4-bit parallel adder (ripple carry) be converted to a parallel subtractor using XOR gates. (Hint: use two's complement subtraction.)
   b) Draw the logic diagram of a three-digit BCD adder and briefly describe its functional principle. (6M+9M)

5. a) How could a 1-of-4 multiplexer plus one other gate be used for the implementation of full adder?
   b) Design a combinational circuit that converts a decimal digit from 2,4,2,1 code to 8, 4,-2,-1code. (6M+9M)
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6. a) Obtain the programming table for the SUM output of the full adder to implement with PLA
   b) What do you understand by the following as regards programmable logic devices?
      i) Combinational and registered outputs;
      ii) Configurable output logic cell;
      iii) reprogrammable PLD; (4M+11M)

7. a) Obtain the count sequence of
      i) a MOD-10 Ring counter
      ii) a MOD-10 Johnson counter
   Determine the number of flip-flops required to construct the above counters.
   b) Draw and explain the operation of universal shift register (8M+7M)

8. a) Convert the following Mealy machine into a corresponding Moore machine?

PS	NS, Z	
	X=0	X=1
A	C,0	B,0
B	A,1	D,0
C	B,1	A,1
D	D,1	C,0

   b) Design the circuit for the above table? (8M+7M)

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1. a) Perform the following operations using 2's complement arithmetic:
   i) $(+43)_{10} - (-53)_{10}$.
   ii) $(3E91)_{16} - (1F93)_{16}$
   b) Represent the unsigned decimal numbers 351 and 986 in BCD, and then show the steps necessary to form their sum. (8M+7M)

2. a) It is proposed to construct an eight-input NAND gate using only two-input AND gates and two-input NAND gates. Draw the logic arrangement that uses the minimum number of logic gates.
   b) What is a parity bit? Define even and odd parity. What is the limitation of the parity code when it comes to detection and correction of bit errors? (8M+7M)

3. a) Use Karnaugh maps to show that $AC + \overline{A}\,\overline{C}$ and $\overline{A}C + A\overline{C}$ are factors of $\overline{A}B\overline{C}D + A\overline{B}\overline{C}D$ and find a suitable third and final factor.
   b) Using the Quine–McCluskey tabular method, find the minimum sum of products for $\sum(1, 2, 3, 9, 13, 14) + \sum_{\phi}(0,7, 10, 15)$ (8M+7M)

4. a) Draw the truth table of a full subtractor circuit. Write a min-term Boolean expression for DIFFERENCE and BORROW outputs in terms of minuend variable, subtrahend variable and BORROW-IN. Minimize the expressions and implement the min hardware.
   b) Briefly describe the concept of look-ahead carry generation with respect to its use in adder circuits. (8M+7M)

5. a) What is a de-multiplexer and how does it differ from a decoder? Can a decoder be used as a de-multiplexer?
   b) Implement the following logic function using MUX with three select inputs?
   $F(a,b,c,d) = \overline{a} + bc\overline{d} + a\overline{d} + c$ (8M+7M)
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6. a) Distinguish between a programmable logic array (PLA) device and a programmable array logic (PAL) device in terms of architecture and capability to implement Boolean functions.

   b) Realize the following switching functions with PROM

   F_1 (A,B,C,D) = ∑m(0,1,3,4,5,6,7,12,13)

   F_1 (A,B,C,D) = ∑m(5,6,7,10,11,13,14,15) (8M+7M)

7. a) Draw the truth table and briefly describe its operation of the following types of flip-flop:

   i) A positive edge-triggered J-K flip-flop with active HIGH J and K inputs and active LOW PRESET and CLEAR inputs;

   ii) A negative edge-triggered J-K flip-flop with active LOW J and K inputs and active LOW PRESET and CLEAR inputs.

   b) Enumerate the differences between transition table and state table? (9M+6M)

8. a) Explain the capabilities and limitations of finite state machines

   b) Convert the following Mealy machine into a corresponding Moore machine. (8M+7M)

PS	NS, Z	
	X=0	X=1
A	B,0	E,0
B	E,0	D,0
C	D,1	A,0
D	C,1	E,0
E	B,0	D,0

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1. a) Solve
   i) $(AD012)_{16} = (X)_5$ ii) $(5.204)_{10} = (X)_3$
   b) Add the maximum positive integer to the minimum negative integer, both represented in
   i) 16-bit 1's complement binary notation. Express the answer in 1's complement binary
   ii) 16-bit 2's complement binary notation. Express the answer in 2's complement binary
   (8M+7M)

2. a) Write both sum-of-products and product-of-sums Boolean expressions for
   i) a two-input AND gate,
   ii) a two-input NAND-gate,
   iii) a two-input EX-OR gate and
   iv) a two-input NOR gate from their respective truth tables.
   b) i) Simplify
   $F(A,B,C,D,E) = ABCD + AB\overline{C}\,\overline{D} + ABC\overline{D} + AB\overline{C}D + ABCDE + AB\overline{C}\,\overline{D}E + AB\overline{C}DE$
   ii) Prove that $[A\overline{B} + \overline{C} + \overline{D}][D + (E + \overline{F})G] = D(A\overline{B} + \overline{C}) + \overline{D}G(E + \overline{F})$ (8M+7M)

3. A logic system has three inputs A, B and C and two outputs Y_1 and Y_2. The output functions Y_1 and Y_2 are expressed by $Y_1 = \overline{A}BC + B\overline{C} + \overline{A}\,\overline{C} + A\overline{B}C + ABC$ *and* $Y_2 = \overline{A}B + A\overline{C} + ABC$
   Determine the minimized output logic functions using the Quine–McCluskey tabular method
   (15M)

4. a) Draw the circuit diagram of a 4-bit adder-subtractor and briefly describe its functional principle.
   b) Briefly describe the concept of look-ahead carry generation with respect to its use in adder circuits. (8M+7M)

5. a) Draw the logic diagram and truth tables for the following:
   i) An eight-line to three-line priority encoder with active LOW inputs and outputs and an active LOW ENABLE input.
   ii) A four-line to16-line decoder with active HIGH inputs and active LOW outputs and an active LOW ENABLE input;
   b) Implement the three-variable Boolean function using an 8-to-1multiplexer and a 4-to-1multiplexer? $F(A,B,C) = \overline{A}C + A\overline{B}C + AB\overline{C}$ (8M+7M)
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6. a) Design four-digit Excess-3 code converter using PROM with the help of programming table
   b) Realize the following switching functions with PAL with the help of programming table
   F_1 (A,B,C,D) = ∑m(0,1,3,4,5,6,7,12,13) (6M+9M)

7. a) How can presettable counters be used to construct counters with variable modulus?
   b) Obtain the count sequence of
      i) a MOD-10 Ring counter
      ii) a MOD-10 Johnson counter
   Determine the number of flip-flops required to construct the above counters. (7M+8M)

8. Convert the following Mealy machine into a corresponding Moore machine and realize using JK Flip-flop (15M)

PS	NS, Z	
	X=0	X=1
A	C,0	B,0
B	A,1	D,0
C	B,1	A,1
D	D,1	C,0